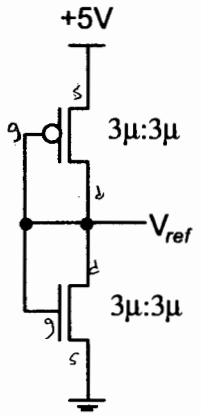
E.E. 451.3 VLSI Circuit Design

ASSIGNMENT #1

Out: January 25th, 2001
Due: February 1st, 2001

The circuit shown below is a voltage reference generator circuit, used to generate auxiliary voltages that might be necessary in certain types of designs (i.e., for pre-charged digital circuits, analog circuits, etc.). It generates an output voltage, V_{ref}, which depends on device parameters, including transistor width and length (W:L).



Determine the output voltage for the circuit shown (size notation is W:L). Use CMOS3DLM device parameters as shown on Page 2. Note that standard substrate connections (not shown) have been made (i.e., VSS for the N-channel transistor and VDD for the P-channel transistor).

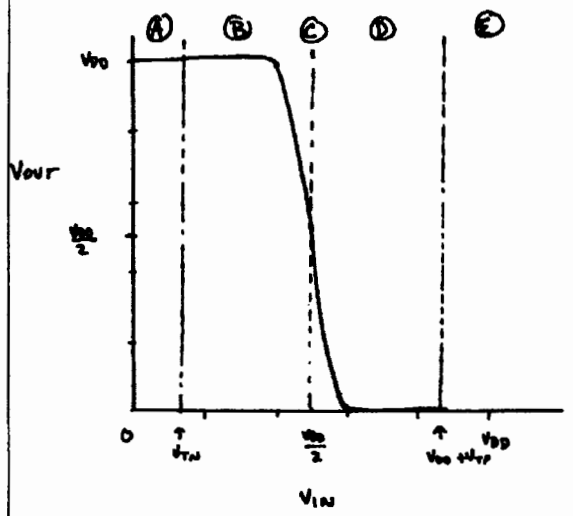
ASSIGNMENT

Q1

FOR CI

AN INV

5 REGIONS



THIS CURVE ASSUMES $\beta_n = \beta_p$

IF $\frac{\beta_n}{\beta_p} > 1$ CURVE MOVES TO LEFT

IF $\frac{\beta_n}{\beta_p} < 1$ CURVE MOVES TO RIGHT

REGION	N-CHANNEL	P-CHANNEL
A	CUT-OFF	LINEAR
B	SATURATED	NON-SATURATED
C	SATURATED	SATURATED
D	NON-SATURATED	SATURATED
E	LINEAR	CUT-OFF

1

PROBLEMS | CLASS (2)
NAME | DATE

EQUATIONS FOR EACH REGION:

(A) $V_{OUT} = V_{DD}$

(B) $V_{OUT} = (V_{IN} - V_{TP}) + \sqrt{(V_{IN} - V_{TP})^2 - 2\left(V_{IN} - \frac{V_{DD}}{2} - V_{TP}\right)V_{DD} - \frac{\beta_N}{\beta_P}\left(V_{IN} - V_{TN}\right)^2}$

(C) $V_{OUT} = \frac{V_{DD}}{2}$

(D) $V_{OUT} = (V_{IN} - V_{TN}) - \sqrt{(V_{IN} - V_{TN})^2 - \frac{\beta_P}{\beta_N}\left(V_{IN} - V_{DD} - V_{TP}\right)^2}$

(E) $V_{OUT} = V_{SS}$

WE KNOW THAT $V_{OUT} = V_{IN}$ IN OUR CIRCUIT. ALSO $\frac{\beta_N}{\beta_P} \approx 3.1$. THEREFORE OUR CURVE IS SHIFTED TO THE LEFT. ALSO WE KNOW THAT WE ARE NOT OPERATING IN REGIONS (A), , OR (E) THEREFORE SOME REGION (B) AND (D) EQUATIONS.

(B) $V_{OUT} = V_{IN} = 0.23\,V$

(D) $V_{OUT} = V_{IN} = 1.98\,V$

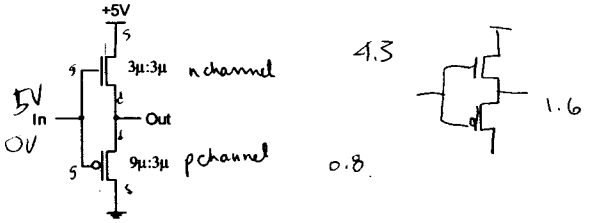
THE CORRECT VALUE IS 1.98 V SINCE 0.23 VOLTS DOES NOT "AGREE" WITH OUR PLOT OF V_{OUT} Vs V_{IN}.
(CHECK WITH HANSPICE: YOU GET SIMILAR VALUE).

E.E. 451.3 VLSI Circuit Design

ASSIGNMENT #2

Out: February 1st, 2001
Due: February 8th, 2001

1. It has been noted that there is no BUFFER gate in CMOS digital logic. Of course a BUFFER can be built using two inverters in series at the expense of added propagation delay and increased size (approximately 2x the size of an inverter). A digital designer has proposed the following circuit as a solution to the BUFFER gate problem. Discuss.



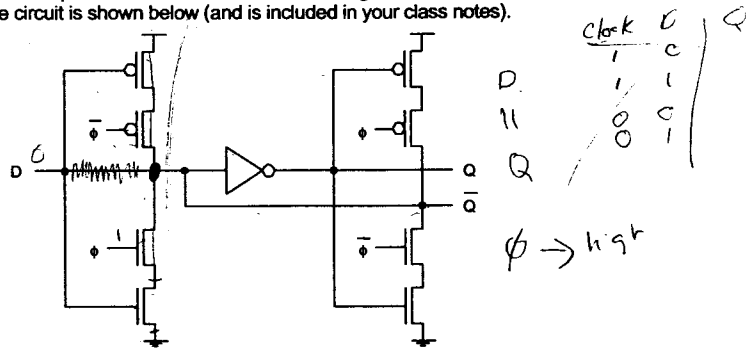
2. Design a CMOS circuit to implement the following logic function.

$$F = \overline{D + A(B + C)}$$

   a. Use only standard NAND, NOR, and INVERTER gates to implement the function. How many transistors are needed?

   b. Use an Arbitrarily Complex Function (ACF) to implement the function. How many transistors are needed?

3. All parts of this question concern a schematic design domain abstraction of a D-type Static Latch. The circuit is shown below (and is included in your class notes).



   a) As mentioned in class, sometimes the design domain abstraction loses track of what the designer intended (reality). Does the circuit function as intended? If not, clearly show your corrected circuit. Verify circuit operation (use a timing diagram).

ASSIGNMENT #2 — EE 451.3 — NAME — DATE — CLASS — ①

Q1

IF $V_{IN} = 5V$ $V_{OUT} = 4.3$ MAX

IF $V_{IN} = 0V$ $V_{OUT} = 0.8$ MIN

THIS IS ASSUMING V_{SB} (SUBSTRATE BIAS; VOLTAGE BETWEEN SOURCE AND BULK) IS 0V. THIS WOULD BE THE CASE IF SOURCE OF N-CHANNEL IS CONNECTED TO V_{SS} AND IF SOURCE OF P-CHANNEL IS CONNECTED TO V_{DD}. THIS IS NOT THE CASE. BOTH SOURCES ARE CONNECTED TO THE OUTPUT. THIS CAUSES A PROBLEM.

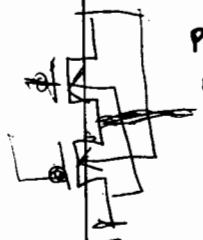
NOW

$$V_T = V_{TO} \pm \gamma\left[\sqrt{2\phi_B + |V_{SB}|} - \sqrt{2\phi_B}\right]$$

FOR N-CHANNEL: $V_{TO} = 0.7V$ $\gamma = 1.1$ use +sign

FOR P-CHANNEL: $V_{TO} = -0.8V$ $\gamma = 0.6$ use −sign

FROM SPICE INFO $2\phi_B = 0.6V$



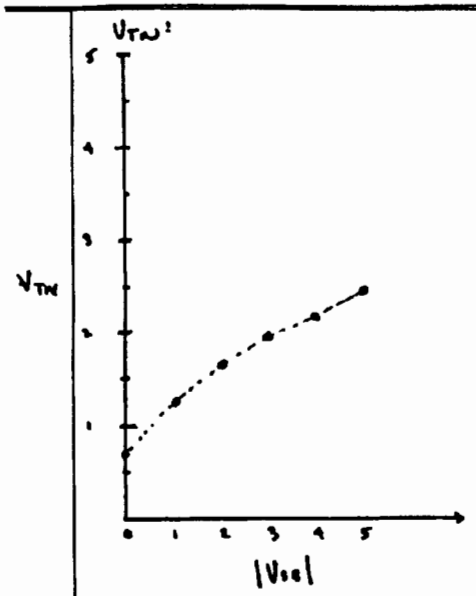
PLUGGING IN THESE VALUES PROVIDES FOLLOWING TABLE

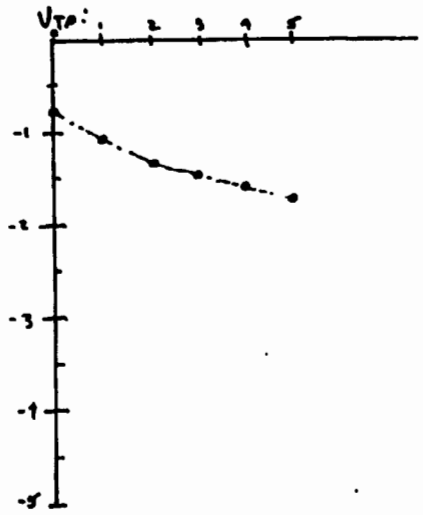
REMEMBER FOR N-CHANNEL $|V_{SB}| = |V_{OUT} - 0|$

P-CHANNEL $|V_{SB}| = |V_{DD} - V_{OUT}|$

V_{OUT}	$\lvert V_{SB}\rvert_N$	V_{TN}	$\lvert V_{SB}\rvert_P$	V_{TP}
0	0	0.70	5	−1.75
1	1	1.29	4	−1.62
2	2	1.62	3	−1.47
3	3	1.93	2	−1.30
4	4	2.21	1	−1.09
5	5	2.96	0	−0.80

PROBLEMS — NAME — DATE — CLASS — ②





NOTE THAT WHEN $V_{OUT} \cong 3V$ $|V_{SB}| = 3$ FOR N-CHANNEL AND $V_{TN} \cong 2V$. THEREFORE THE N-CHANNEL TRANSISTOR IS ENTERING CUT-OFF.

SIMILARLY WHEN $V_{OUT} \cong 1.5V$ $|V_{SB}| = 3.5$ FOR P-CHANNEL AND $V_{TO} \cong 1.5V$. THEREFORE THE P-CHANNEL TRANSISTOR IS ENTERING CUT-OFF

THEREFORE OUTPUT SWING IS LIMITED TO

$1.5V \leftrightarrow 3.0V$ (APPROXIMATELY)

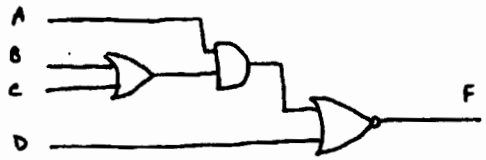
THIS IS NOT VERY GOOD.

(NOTE: CHECK WITH WINSPICE. YOU GET SIMILAR VALUES)

"If you say by inspection, I won't believe you. On an exam I am going to wonder how you got MAPLE to work when you left to go to the toilet."

Q2: $F = \overline{D + A(B+C)}$

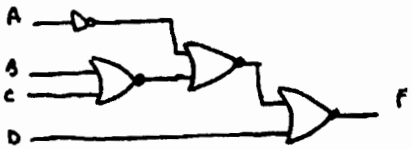
IF WE JUST GO AHEAD AND USE AND, OR, INVERTERS: (LITERAL IMPLEMENTATION)



WE USE 2 (3 TRANSISTORS) + 1 (4 TRANSISTORS)
= 16 TRANSISTORS

IF WE USE BOOLEAN ALGEBRA TO SIMPLIFY EQUATION INTO NAND, NOR, INVERTER FORM.

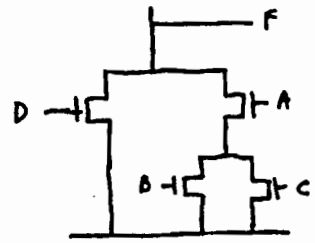
$F = \overline{\overline{D + A' + (B+C)}}$



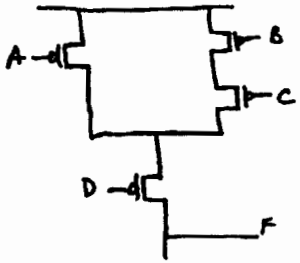
WE USE 3(4 TRANSISTORS) + 1(2 TRANSISTORS)
= 14 TRANSISTORS

<u>HOWEVER</u> IF WE USE AN ACF AND REALIZE THAT F IS A COMPLEMENTED FUNCTION:

PULL DOWN CIRCUIT IS



THEREFORE PULL-UP CIRCUIT IS:



TOTAL NUMBER OF TRANSISTORS IS

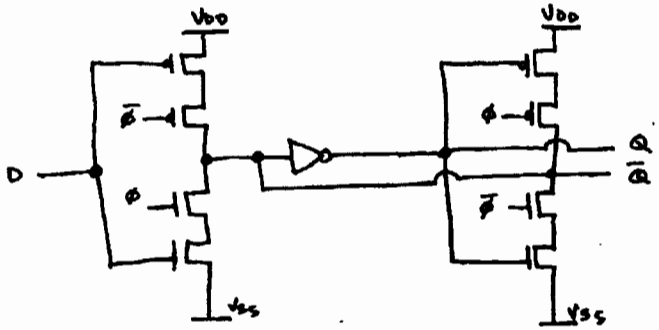
4 + 4 = <u>8</u>

"Good morning. I hate 8:30 classes, but not you personally."

NAME DATE (5)

Q3: THE CIRCUIT DOES NOT FUNCTION AS INTENDED. THE FIRST STAGE CLOCKED-INVERTER DOES NOT HAVE ITS OUTPUT CONNECTED TO ANYTHING. THIS IS BECAUSE THE D INPUT GOES DIRECTLY TO THE INVERTER INPUT.

CORRECT CIRCUIT IS:



NOTE THAT Q CAN "FOLLOW" D DEPENDING ON ϕ AND $\bar{\phi}$. THUS IT IS A LATCH.

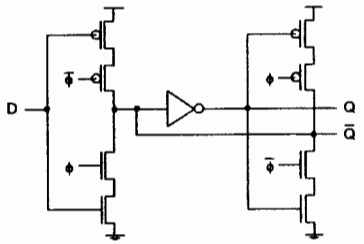
THERE ARE NUMEROUS RIGHT TIMING DIAGRAMS. JUST REMEMBER THAT ϕ AND $\bar{\phi}$ ARE INTENDED TO BE GATE SIGNALS, THEREFORE D SHOULD CHANGE AT A SLOWER FREQUENCY.

E.E. 451.3 VLSI Circuit Design [redacted]

ASSIGNMENT #3

Out: February 15th, 2001
Due: March 8th, 2001

1. All parts of this question concern a schematic design of a D-type Static Latch. The correct circuit is shown below.



A library of standard cells (Assignment_3.elib) is on the E.E. 451.3 class web-site (http://www.engr.usask.ca/classes/EE/451) linked off of the assignment page. Save this library where you are working on this assignment. This library contains an inverter and a design for a clocked inverter (clk_inv) for your use. If you are using an Apple computer, please see me.

a) Using the standard cells in the provided library "wire together" the above circuit using Electric. Obtain a print out of your layout plot.

b) Perform a logic simulation using the ALS simulator built into Electric (**Tools->Simulation->Simulate...**). Obtain a print out of your timing plot.

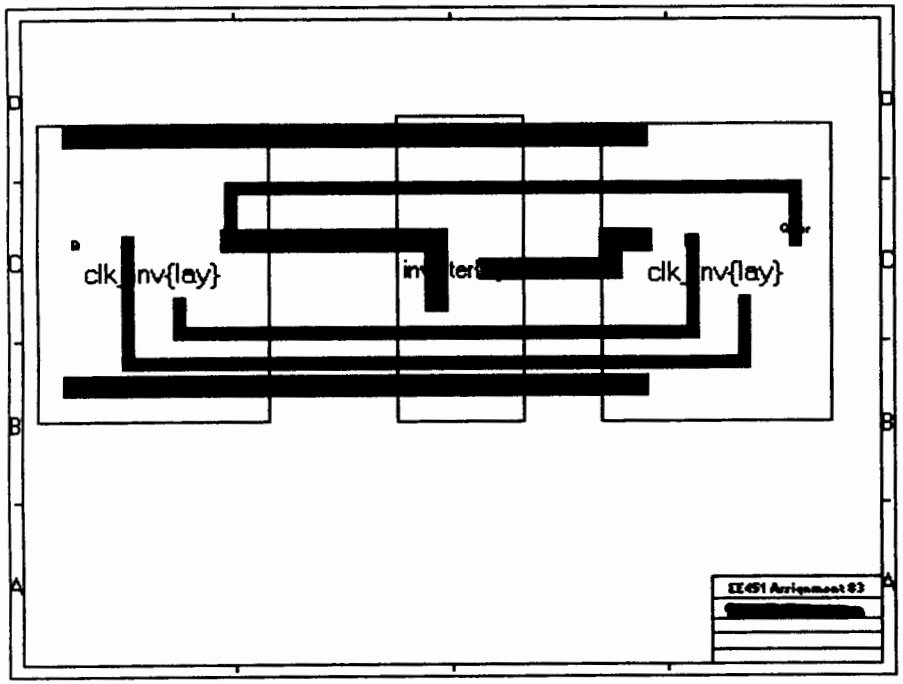
Engineering Physics student please note:

Accessing Electric and Winspice from domains other than Engineer

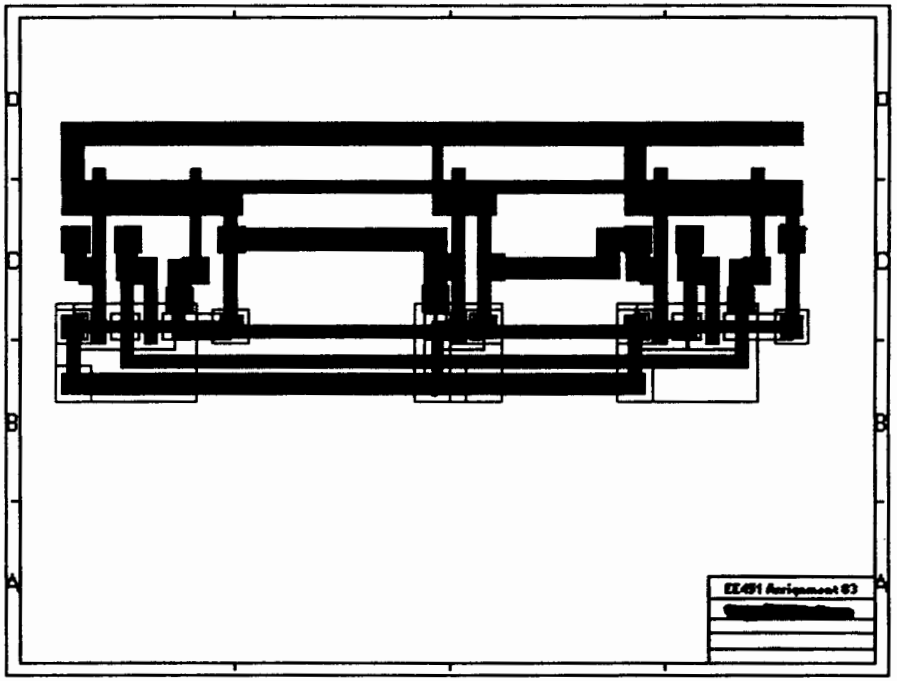
Electric and WinSpice should be available by copying them from the PROGRAMS folder in the winapp folder on the computer named RUBE in the Engineer domain accessed from the Network Neighborhood shortcut usually found on the desktop of the PCs. Please note that they are relatively large.

Engineer domain: \\RUBE\winapp\\PROGRAMS\electric

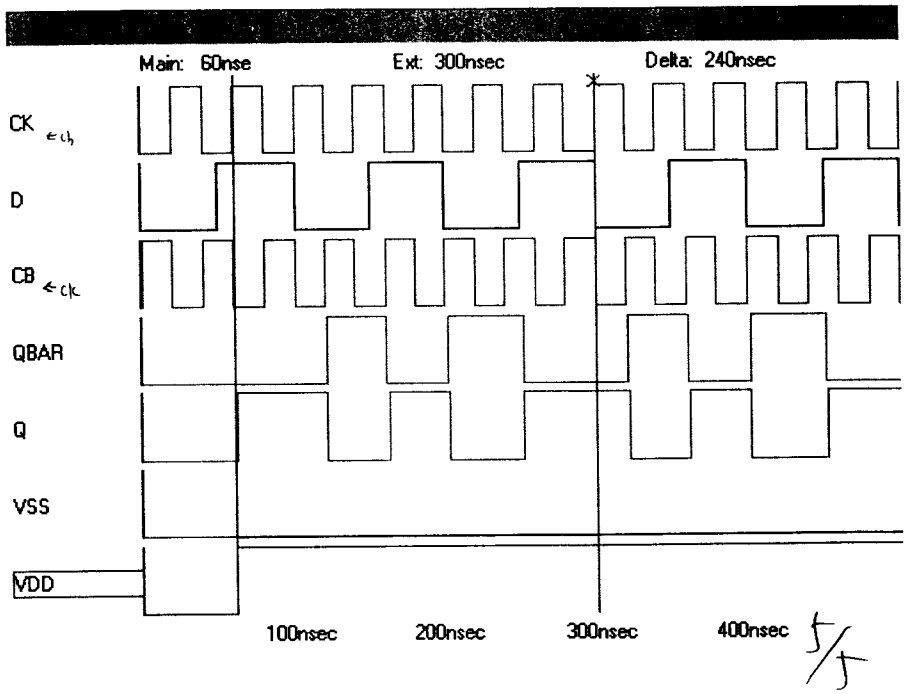
Engineer domain: \\RUBE\winapp\\PROGRAMS\winspice



Best to use the next page.



"Put up your hands if this makes sense." (one hand goes up) "Good enough."

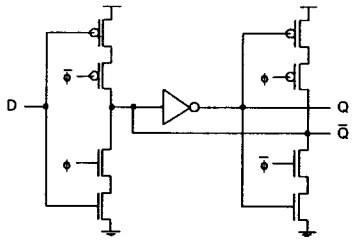


E.E. 451.3 VLSI Circuit Design

ASSIGNMENT #4

Out: March 8th, 2001
Due: March 15th, 2001

1. All parts of this question concern a schematic design of a D-type Static Latch. The correct circuit is shown below.



A library of standard cells (Assignment_3.elib) is on the E.E. 451.3 class web-site (http://www.engr.usask.ca/classes/EE/451) linked off of the assignment page. Save this library in the directory where you are working on this assignment. This library contains an inverter and a design for a clocked inverter (clk_inv) for your use. If you are using an Apple computer, please see me.

a) Using your circuit from Assignment #3, extract the SPICE deck for the s-latch and simulate using WinSpice. Use the same signals as you used in Assignment #3. Obtain a print out of your SPICE plot.

If you are adding SPICE parts to your s-latch layout using Electric (**Edit->New SPICE Part...**) you will have to add the following:

- A Voltage Source for the vdd power supply (DC 5)
- A Voltage Meter on both the Q and Qbar outputs.
- Some form of clocked Voltage Source on the ck and cb inputs. Usually a PULSE signal is used. Make sure times are in n (for nano) seconds.
- Some form of "clocked" Voltage Source on the D input. Usually a PULSE signal is used. Make sure times are in n (for nano) seconds.
- A Transient analysis part to set the SPICE deck up for a timing type of analysis. Use 0.1n 500n.

Engineering Physics student please note: Electric and WinSpice should be available by copying them from the Winapp directory on the computer named Rube in the Engineer domain accessed from the Network Neighborhood.

```
** FACET s-latch FROM LIBRARY ass3 ***
** FACET CREATED Tue Mar 06 17:56:37 2001
** VERSION 1 LAST REVISED Wed Mar 07 12:08:57 2001
** EXTRACTED BY ELECTRIC DESIGN SYSTEM, VERSION 5.7.3
** UC SPICE *** , MIN_RESIST 50.000000, MIN_CAPAC 0.040000FF
.OPTIONS NOMOD NOPAGE
* Northern Telecom 3 Micron CMOS PROCESS
* Models Taken From CMC Document GICIS 3.0, January 1987
* Parameters expressed in terms of real microns

.OPTIONS DEFL=3UM DEFW=3UM DEFAS=60PM DEFAD=60PM
+ LIMPTS=20000 ITL3=10 ITL4=30 ITL5=40000
+ LVLTIM=2  ITL6=30 METHOD=TRAP GMIN=1.E-10
+ ABSTOL=10PA VNTOL=10UV

.MODEL N NMOS ( LEVEL=1 VTO=0.7 KP=40E-6 GAMMA=1.1 PHI=0.6
+ LAMBDA=1.0E-2 PB=0.7 CGSO=3.E-10 CGDO=3.E-10 CGBO=5.0E-10
+ RSH=25 CJ=4.4E-4 MJ=0.5 CJSW=4E-10 MJSW=0.3 JS=1.0E-5
+ TOX=5.0E-8 NSUB=1.7E+16 TPG=1 XJ=6.0E-7 LD=3.5E-7 UO=775 )

.MODEL P PMOS ( LEVEL=1 VTO=-0.8 KP=12.E-6 GAMMA=0.6 PHI=0.6
+ LAMBDA=3.0E-2 PB=0.6 CGSO=2.5E-10 CGDO=2.5E-10 CGBO=5.0E-10
+ RSH=80 CJ=1.5E-4 MJ=0.6 CJSW=4.E-10 MJSW=0.6 JS=1.0E-5
+ TOX=5.0E-8 NSUB=5.0E+15 TPG=1 XJ=5.E-7 LD=2.50E-7 UO=250 )


.SUBCKT clk_inv a z vdd ck cb
* POWER NET: vdd
* GROUND NET: 0 (gnd)
* PORT a (network: a)
* PORT z (network: z)
* PORT vdd (network: vdd)
* PORT ck (network: ck)
* PORT cb (network: cb)
Mode6 z cb net2 vdd P L=3.00U W=9.00U AS=97.20P AD=91.80P PS=30.60U
+ PD=38.40U
Mode7 net2 a vdd vdd P L=3.00U W=9.00U AS=70.20P AD=97.20P PS=33.60U
+ PD=30.60U
Mode10 net1 a 0 0 N L=3.00U W=3.00U AS=36.36P AD=15.30P PS=26.40U PD=13.20U
Mode11 z ck net1 0 N L=3.00U W=3.00U AS=15.30P AD=77.76P PS=13.20U PD=54.00U
* Extracted Parasitic Elements:
C1 a 0      11.39F
C2 ck 0       9.80F
C3 vdd 0      11.91F
C4 z 0       7.39F
C5 cb 0      10.06F
.ENDS clk_inv

.SUBCKT inverter a z vdd
* POWER NET: vdd
* GROUND NET: 0 (gnd)
* PORT a (network: a)
* PORT z (network: z)
* PORT vdd (network: vdd)
Mode7 z a 0 0 N L=3.00U W=3.00U AS=75.96P AD=36.36P PS=52.80U PD=26.40U
Mode10 z a vdd vdd P L=3.00U W=9.00U AS=104.76P AD=70.20P PS=62.40U
+ PD=33.60U
* Extracted Parasitic Elements:
C1 vdd 0       3.06F
C2 a 0      12.18F
C3 z 0       7.39F
.ENDS inverter

** TOP LEVEL FACET: s-latch{lay}
* POWER NET: Vdd
* GROUND NET: 0 (Vss)
* PORT Qbar (network: Qbar)
* PORT Q (network: Q)
* PORT ck (network: ck)
* PORT Vdd (network: Vdd)
* PORT D (network: D)
* PORT cb (network: cb)
Xmodel1 D Qbar Vdd ck cb clk_inv
Xmode2 Q Qbar Vdd cb ck clk_inv
Xmode3 Qbar Q Vdd inverter
```

EE451
Assignment #4

[redacted]

[redacted]

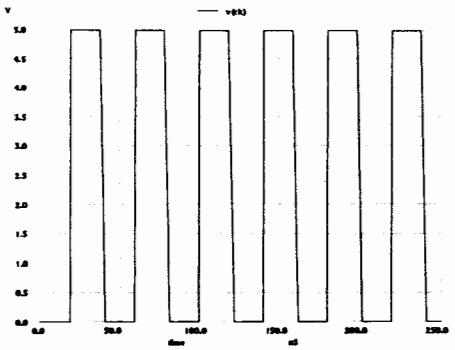
10/10

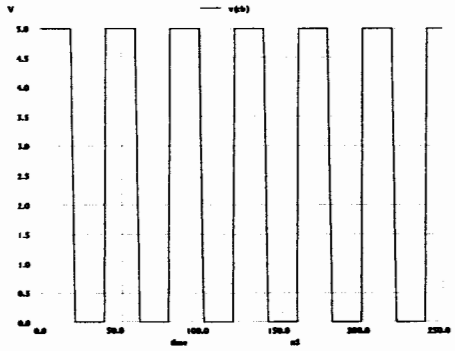
[redacted] Added code *

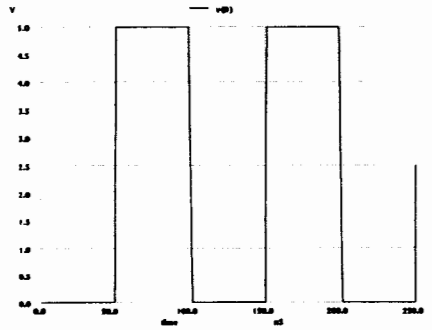
```
** Extracted Parasitic Elements:
C1 Vdd 0      33.90F
C2 Q 0       11.68F
C3 ck 0       13.60F
C4 cb 0       17.04F
C5 Qbar 0      31.18F
.END
```

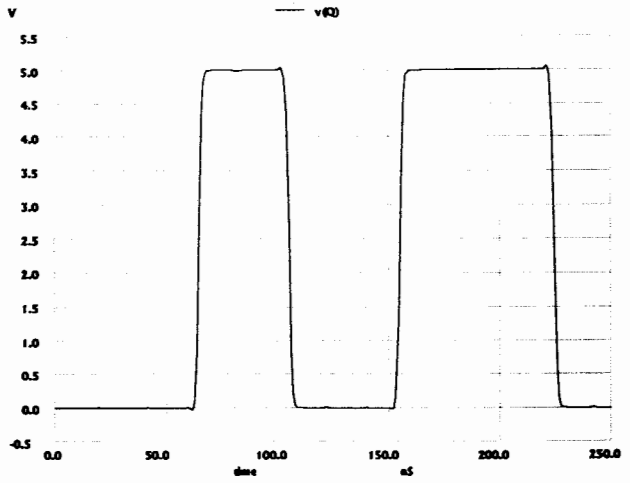
* Added code is:

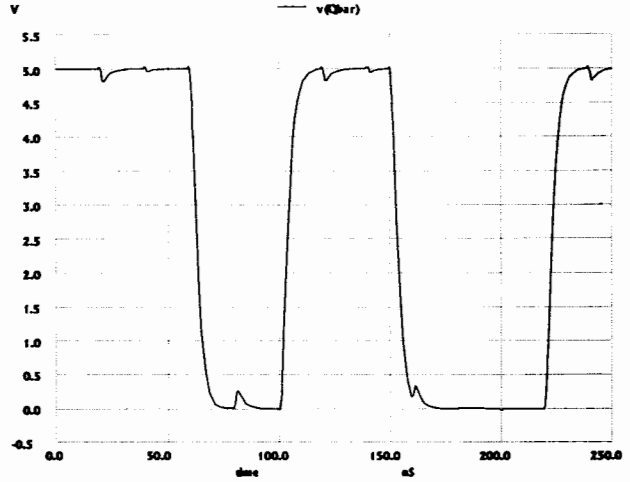
```
VIN ck 0 pulse(0 5 19NS 2NS 2NS 18NS 40NS)
VIN1 cb 0 pulse(5 0 19NS 2NS 2NS 18NS 40NS)
VCC VDD 0 DC 5
VIN2 D 0 pulse(0 5 49NS 2NS 2NS 48NS 100NS)
VCC1 GND 0 DC 0
.print tran V(Q) V(Qbar)
.tran 0NS 250NS .1NS
```







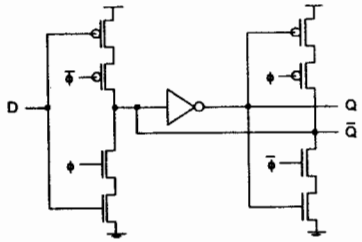




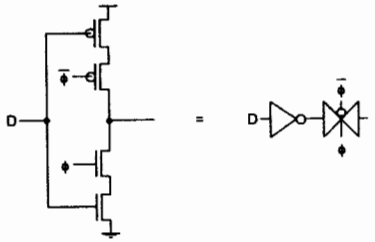
ASSIGNMENT #5

Out: March 20th, 2001
Due: March 29th, 2001

1. All parts of this question concern a schematic design of a D-type Static Latch. The correct circuit is shown below.



a) Write the structural VHDL code necessary to implement the above circuit. Note that a clk_inv standard cell does NOT exist in the NC3LIB standard cell library (i.e., cmos3dlm.txt). Therefore you will have to make one out of an inverter standard cell followed by a tgate (i.e., transmission gate) standard cell. See circuit below. Use as much hierarchy as possible in your design. Assume that you have a single-phase clock available and that you have to generate the two-phase clock.




```
-- Design of D-Type Static Latch
-----------------------------------------------------------
[redacted]
-----------------------------------------------------------

-- Top Level Interface
-----------------------------------------------------------
ENTITY D_Static_Latch IS
PORT (D, CLK: IN BIT; Q, QB: OUT BIT);
END;

-----------------------------------------------------------
--Architecture of D_Static_Latch
-----------------------------------------------------------
ARCHITECTURE D_Static_Latch_body of D_Static_Latch is
        COMPONENT Clocked_Inverter PORT (A, CK, CB: IN BIT; Z: OUT BIT);
        END COMPONENT;
        COMPONENT twophase PORT (inphi: IN BIT; phi, phibar: OUT BIT);
        END COMPONENT;
        COMPONENT Inverter PORT(A: IN BIT; Z: OUT BIT);
        END COMPONENT;
        SIGNAL phi, phibar: BIT;

BEGIN
Two_Phase_Clk : twophase PORT MAP (CLK, phi, phibar);
Inverter_1:  Inverter PORT MAP (QB, Q);
Clkd_Inverter_1: Clocked_Inverter PORT MAP (D, phi, phibar, QB);
Clcd_Inverter_2: Clocked_Inverter PORT MAP (Q, phibar, phi, QB);
END;

-----------------------------------------------------------
-- Clocked_Inverter
-----------------------------------------------------------
ENTITY Clocked_Inverter IS
PORT (A, CK, CB: IN BIT; NotA: OUT BIT);
END Clocked_Inverter;

-----------------------------------------------------------
--Architecture of Clocked_Inverter
-----------------------------------------------------------
ARCHITECTURE Clocked_Inverter_body of Clocked_Inverter is
        COMPONENT Inverter PORT(A: IN BIT; NotA: OUT BIT);
        END COMPONENT;
        COMPONENT tgate PORT(CK, CB, A, B: IN BIT);
        END COMPONENT;
        SIGNAL Alena: BIT;

BEGIN
Inverter_too:  Inverter PORT MAP (A, Alena);
Fence: tgate PORT MAP (CK, CB, Alena, NotA);
END;
```

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